in an ECC to be processed.

The odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making the bus control means start a concurrent data transfer not at the head but at the code word of the sector from which an error-containing code has been detected, based on the information designated by the non-error sector code word range designating sub means; for making the syndrome calculating means start syndrome calculation at the code word; and for making the error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in the storing means as an initial value.

In the aspect 10, in the error correction devices of the aspects 7 and 8 further comprising a sector-basis storing means for storing mid-term results, on a sector-by-sector basis, in code word units, of each code word from which no error has been detected in the error detecting process done by the error detecting means, until the syndrome calculating means detects an error-containing code. As a result, the same action as in the aspect 9 is done in code word units of each sector.

In the aspect 11, in the error correction devices of the aspects 7 and 8 further comprising a sector-group-basis storing means for storing mid-term results, on a sector-group-by-sector-group-basis, in code word units, of each code word from which no error has been detected in the error detecting process done by the error detecting means until the syndrome calculating means detects an error-containing code. As a result, the same action as in the aspect 9 is done in code word units of each sector.

In the aspects 12-15, in the error correction devices of the aspects 1, 2, 5, 6, 7, and 8, error correction is performed in parallel (by means of so-called pipeline processing) for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction, for example a sector as a unit, are subjected to the error correction.

The buffer memory is a plural-ECC-block-division buffer memory for storing a plurality of ECC blocks to be processed in parallel by assigning addresses either sequentially or like a circle conceptually in pipeline processing, and for reading data in the same manner.

The storing means for storing mid-term results of an error detecting process generated by the error detecting means is an ECC-block-division storing means for storing the plurality of ECC blocks on a block-by-block basis.

In the system control means, the means-basis ECC block pipeline processing notification sub means transmits one or more ECC blocks which have been subjected to error correction downstream; stores one or more ECC blocks to be processed next at a predetermined address such as the address of the ECC block transferred downstream by overwriting them in the plural-ECC-block-division buffer memory; and makes the storage known to the bus control means, the syndrome calculating means, the error

detecting means, and the error correcting means. To be more specific, the table showing processing targets referred to by each means are re-written. Besides, in the downstream units, transferred ECC blocks may be rearranged in accordance with the original order.

The means-basis ECC block recognition sub means recognizes a data transfer from the bus control means to the syndrome calculating means, to the error detecting means, and to the error correcting means for error detection and error correction; recognizes the error correction done by the error correcting means; recognizes writing of error-corrected data to the plural-ECC-block-division buffer memory done by the bus control means; recognizes ECC blocks in process when the error detecting means stores mid-term results to the plural-ECC-block-division storing means, and selects ECC blocks to be processed.

The ECC block notification sub means in sub means-basis pipeline processing notifies the first error detecting sub means, the even-numbered error correction sub means, the odd-numbered error correction sub means, the number-of-times control sub means, and the DMA transfer instruction sub means contained in the system control means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in the plural-ECC-block-division buffer memory, and further notifies these same sub means contained in the system control means of the ECC blocks which are in process therein.

In the aspects 16-19, in the error correction devices of aspects 1, 2, 5, 6, 7, 8, 9, 10, and 11, error correction is performed in parallel for a plurality of ECC blocks according to pipeline processing as follows.